High performance PSR power switch IC

1. Feature

Built-in TruePSR™ high-precision sampling technology
Built-in 650 V high voltage NMOSFET switch
Precise primary side regulation accuracy is better than 2%
Precise primary side constant current accuracy is better than 3%
Built-in fixed output voltage drop compensation range is 3.2%
Low switching loss with full valley switch mode
Low standby consumption and high energy efficiency to meet the CoC V5 & DoE VI requirements
No-load standby power consumption as low as 50 mW or less
Built-in CT-PSR™ active cycle tuning technology
Low-frequency start-up characteristic control optimizes the starting performance
Highly reliable low EMI gate drive with soft clamp
Built-in output over-voltage, short circuit and over-load protection
Optimized full-range audio-free operation
SOP8 package with high isolation distance and reasonable layout

2. Applications

IT Equipment Charger
Power Adapter
Battery Charger
Open-frame Power

3. Description

The LN1F16/17/18/19/19A/19B is a new generation of high-performance, highly integrated current-mode PSR power switch ICs that can easily build low-standby power consumption, high conversion efficiency, and low power dissipation to meet the energy efficiency standards of CoC V5 and DoE LEVEL VI in applications up to 45 W with LiiSEMI's sync-rectifier ICs LN5Sxx, High-performance PSR primary side of the CC / CV switching power supply solutions. The chip has built-in high precision constant current and constant voltage control and has an optimized valley switch technology that provides output current error of better than ± 3% accuracy and ± 2% accuracy of output voltage error over the full range.

Switching frequencies of up to 70 kHz allow the use of relatively small transformer size to complete the design, while a very small dead-time control allows the system to work in close to critical conduction mode to improve the utilization of the transformer, far superior to traditional PSR controller architecture.

With PWM / PFM / PBM mode multi-segment curve control mode of operation can further optimize the system under different load conversion efficiency, especially at light load conversion efficiency, very light load conditions will automatically lock the peak current threshold to maintain efficient conversion, segmented modulation design makes the system with high

conversion efficiency while effectively avoiding audible noise, the standby power consumption can be as low as 50 mW the following.

The low-frequency start-up feature automatically operates once during per turn-on and system reset to optimize startup characteristics and effectively reduce the impact on the high-voltage power switch when switching on and off. Soft-clamp gate drive control further removes high, while the active gate slope control significantly improves the level of switching interference. The new generation of cycle-rotation technology for PSR architecture makes the system extremely EMI-friendly.

The chip can also compensate for the output voltage drop through a specially designed linear output cable voltage drop compensation fixed to improve the accuracy of the output voltage under load and maintain accurate load voltage from the load. The internal fixed compensation range is 3.2%, for example, a 5 V output system with a maximum compensation voltage of approximately 0.16 V.

LN1F16/17/18/19/19A/19B also provides a very complete protection circuit with automatic recovery, including cycle-by-cycle current limit (OCP), with high and low voltage compensation output overcurrent protection (OCP), VDD over-voltage protection and under voltage lockout (UVLO) .

Now halogen-free SOP8 standard green packaging is available.

4. Functional Block Diagram

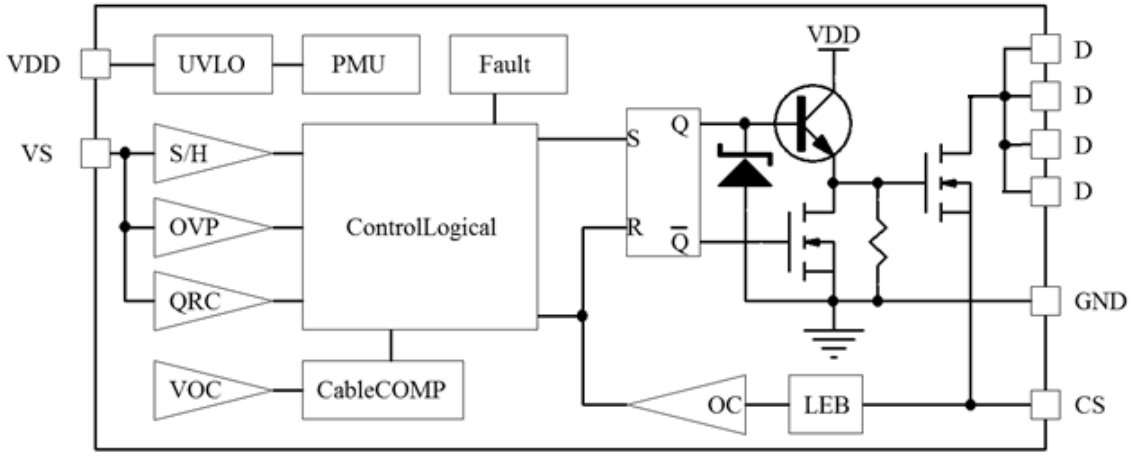

Fig1. Internal functional block diagram

5. Pin Definitions

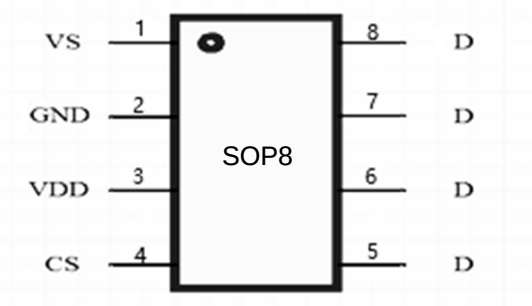

Fig2. Pin Definitions

6. Pin Function Description

PIN	Symbol	Function
1	VS	Output voltage and switch signal detection pin, connected to the feedback sampling network
2	GND	Ground pin
3	VDD	Power supply pin, connect the starting resistor and auxiliary power supply circuit
4	CS	Switch current sense signal input pin, connected to the current sense resistor
5/6/7/8	D	The high-voltage MOSFET switch's drain output pin, which connects the transformer

7. Typical Simplified Schematic

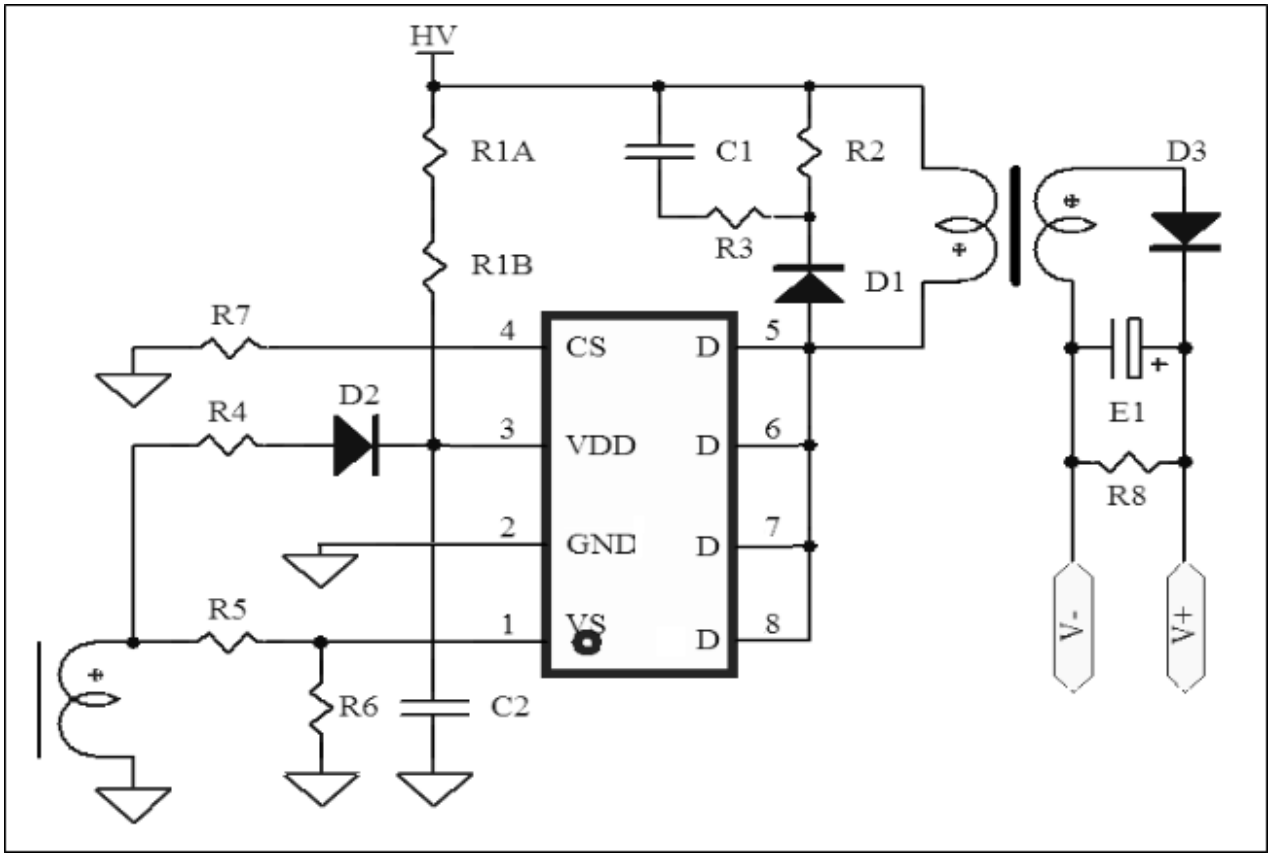

Fig3. Typical Simplified Schematic

8. Absolute Maximum Ratings *

Item		Parameter	unit
D Pin Voltage		650**	V
VDD Pin Voltage		30***	V
Other Pin Voltage		-0.3 to +7	V
D Pin Current (LN1F16)		1****	A
D Pin Current (LN1F17)		2****	A
D Pin Current (LN1F18)		3****	A
D Pin Current (LN1F19)		4****	A
D Pin Current (LN1F19A)		6****	A
D Pin Current (LN1F19B)		9****	A
Min/Max Operation Junction Temperature T_J		-40 to +150	℃
Min/Max Operating Ambient Temperature Ta		-20 to +125	℃
Min/Max Storage Temperature Tstg		-55 to +150	℃
PD		1200	mW
ESD	HBM	2500	V
	MM	250	V

Note*: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for ex tended periods may affect device reliability.** : with 1mA limit. *** : with 10mA limit. ****: For test, Pulse width is 1ms and cycle is 1S.

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9. Recommended Operating Conditions

Symbol	Parameter	Min	Type	Max	Unit
VDD	VDD Voltage	9	13	25	V
FS	Switch frequency		55	65	KHz
Ip	D Ipeak LN1F16			0.35	A
Ip	D Ipeak LN1F17			0.70	A
Ip	D Ipeak LN1F18			1.05	A
Ip	D Ipeak LN1F19			1.40	A
Ip	D Ipeak LN1F19A			2.25	A
Ip	D Ipeak LN1F19B			3.35	A
TA	Operating ambient temperature	-20		85	℃

10. Electrical Characteristics(Ta = 25℃, VDD=15V, if not otherwise noted)

MOSFET Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Voltage	VDD=0V,I_D=1mA	650	700		V
I_{HV}	D-S leakageCurrent	V_D=650V			10	uA
$R_{DS}ON$	MOSFET RdsON	I_D=0.35A,T_J=25℃,LN1F16		7.5	11	Ω
		I_D=0.55A,T_J=25℃,LN1F17		4.3	5.0	Ω
		I_D=0.75A,T_J=25℃,LN1F18		3.3	3.8	Ω
		I_D=1.00A,T_J=25℃,LN1F19		2.1	2.4	Ω
		I_D=1.50A,T_J=25℃,LN1F19A		1.5	1.7	Ω
		I_D=2.00A,T_J=25℃,LN1F19B		0.95	1.1	Ω
T_R	Switch Rise Time	CL=1mH		50		nS
T_F	Switch FallTime	CL=1mH		100		nS
I_D	Drain Current Pulsed	LN1F16, T_J=25℃		1		A
		LN1F16, T_J=105℃		0.5		A
		LN1F17, TJ=25℃		2		A
		LN1F17, TJ=105℃		1		A
		LN1F18, TJ=25℃		3		A
		LN1F18, TJ=105℃		1.5		A
		LN1F19, TJ=25℃		4		A
		LN1F19, TJ=105℃		2		A
		LN1F19A, TJ=25℃		6		A
		LN1F19A, TJ=105℃		3		A
		LN1F19B, TJ=25℃		9		A
		LN1F19B, TJ=105℃		4.5		A

VDD Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{QS}	VDD startup current	VDD=20V	-	1	10	uA
I_Q	Operating current	VDD=16V,VFB=OPEN	-	0.5	-	mA
V_{STOP}	UVLO Threshold voltage	VDD=25V à 0V	7.8	8.8	9.8	V
V_{START}		VDD=0V à 25V	-	21	-	V
V_{OVP}	VDD OVP Threshold	I_{VDD}=5mA	-	27.5	-	V
VDD_CL	VDD Clamp Voltage	I_{VDD}=10mA	-	30	-	V

VS Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CV}	VS reference voltage		4.00	4.05	4.10	V
V_{VSOVP}	VS OVP threshold			5.00		V
G_{OCC}	OCC Scale by Vout	Load=Max Load		3.2		%
V_{OCC}	OCC Voltage	For Vout=5V,Max load		0.16		V

CS Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{LEB}	L.E.B Time			250		nS
Z_{CS}	CS Input Resistance			40		KΩ
T_{OCP}	OCP Delay Time	VDD=16V,CS>VTH_OC		75		nS
V_{THOCPH}	Max. OCP Threshold			0.75		V
V_{THOCPL}	Min. OCP Threshold			0.20		V
V_{THOSP}	OSP Thresholdvoltage			1.45		V

OSC Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{OSC}	Switching Frequency	BurstMode Not entered	22		70	kHz
F_{OSCMIN}	Min. Switching Frequency	BurstMode enter		300		Hz
ΔF_{OSC}_T	F_{OSC} VS Ta	VDD = 16V,Ta=-20℃ to 100 ℃		5		%
ΔF_{OSC}_V	F_{OSC} VS VCC	VDD = 12-25V		5		%
D_{Max}	Max. Duty	VS < 4V		50		%
T_{DIS}_Min	Min. Discharge Time			2		us

Cycleturning™ II (C.T.II) Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ΔF_{OSC}	C.T. range		-2		+2	%
T_{CT}	C.T. time		-	4	-	mS

OTP Section

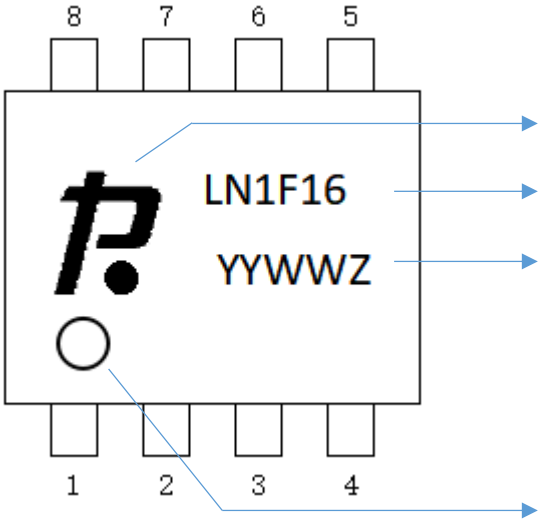
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{OTP}	OTPThreshold		-	150	-	℃
t_{OTPHYT}	OTPHysteresis		-	30	-	℃

Thermal Data

Symbol	Parameter	Rating	Unit
θ_{JA}[1]	Thermal Resistance Junction-Ambient	60	℃/W
θ_{JC}[2]	Thermal Resistance Junction-Case	20	℃/W

Notes: 1. All leads are soldered on a 250mm^2 copper foil with 2oz thick to measuring. 2. Measured on the surface of the package near pin 5/6/7/8.

11. Marking Information



LII SEMICONDUCTOR Trademark logo

Part Number, LN1F16~19B

DateCode：

YY: YEAR, E.g. 20 is 2020;
WW: Week, E.g. 01~52 ;
Z: Other production auxiliary information, etc.

PIN1 location mark

12. Application and Implementation

The LN1F16/17/18/19/19A/19B is a highly integrated, constant-current, constant-voltage PSR controller IC optimized for off-line applications below 20 W. Its highly efficient BM and valley switch hybrid mode control significantly reduces standby losses, improves conversion efficiency at light loads, and easily meets international energy efficiency standards such as CoC V5 and DoE LEVEL VI energy efficiency

12.1 Start-up current and start-up control

The LN1F16/17/18/19/19A/19B can operate at very low start-up current conditions, with accurate UVLO control enabling fast and reliable power-up in a short period of time. Allowing a large start-up resistor value can significantly reduce the start-up power consumption, such as 4MΩ, although a 1/8W power-class resistor can meet the required power requirements, but must still carefully consider its ability to withstand voltage, The use of resistors in series is recommended, for example, using two 1206-type chip resistors in series.

The start-up resistor can be connected between the positive or AC input terminal of the input DC high voltage and the VDD storage capacitor. When the VDD voltage is charged to 21V after power-on, the internal circuit is started and the output drive pulse is finally set to GATE terminal, the system work begins.

12.2 Operating Current and VDD Capacitance

LN1F16/17/18/19/19A/19B the normal operating current as low as 0.8mA, the IC itself when the loss is small, a capacity of not less than 3.3uF capacitor to meet the IC power supply and drive enough energy to consider the larger MOSFET input capacitance and wide Of the operating temperature range, should choose a lower internal resistance (ESR) of the capacitor type to open the MOSFET to provide fast and large current to speed up the MOSFET turn-on, in a typical system design recommended 4.7uF capacitor as VDD capacitance. In order to meet the maximum operating conditions of the VDD range, the capacitor voltage should be not less than 35V better. The effect of noise can be further reduced by connecting a non-polar capacitor in parallel to the VDD pin.

12.3 Cycleturning™ PSR (C.T. PSR)

The LN1F16/17/18/19/19A/19B incorporates a proprietary, second-generation CycleTurning™ technology optimized for PSR that is clocked at the set time (CT-PSR) for the duration of the work cycle, resulting in a larger switching pulse spectrum，to reduce the narrowband energy density, so that any single bandwidth within the average interference intensity greatly reduced. Therefore, the cost of the system in the EMI is greatly reduced.

12.4 Extended BM operating characteristics

The MOSFET switching loss ratio will increase significantly; while the switching loss and switching frequency is proportional to the lower switching frequency can significantly reduce the MOSFET switching losses. LN1F16/17/18/19/19A/19B by detecting the VS voltage and time size, the system no-load or light load will automatically adjust the switching frequency to a lower value, the more the internal modulation voltage is lower than the set control voltage, the more the frequency will decrease, but the circuit will automatically limits the minimum value of the frequency drop above 22kHz to avoid audible

noise.

When the system frequency drops to near 22KHz, if the modulation voltage is still lower than the set control voltage, the output will be disabled to ensure that the output voltage will not be too high, then the system will enter the BM mode to avoid audio noise, and as the load continues to reduce the number of pulses until the pulse into a single state, in order to optimize the system dynamic load response performance, the system will automatically lock the lowest equivalent switching frequency of 300Hz.

12.5 Current detection and leading edge blanking

The LN1F16/17/18/19/19A/19B provides cycle-by-cycle current limiting, and the switching current is sampled into the IC through the current limiting resistor. The built-in leading-edge blanking eliminates current spikes into the IC, preventing current limiter malfunctions and preventing MOSFETs from being faulted, thus eliminating the need for a conventional external blanking circuit.

The maximum current limit threshold, the current comparator's maximum threshold voltage is 0.75V.

12.6 Constant voltagecontrol

LN1F16/17/18/19/19A/19B by sampling the voltage waveform on the auxiliary winding, through a series of sampling, holding, analysis, and processing inside the chip, various signals are generated. Which compares the voltage signal with the internal reference voltage to generate a voltage error signal and adjusts the switch state according to the voltage error signal so as to compensate for the increase or decrease of the output load and the change of the output voltage caused by the increase or decrease of the input voltage, The typical output voltage (Vout) is:

$$V_{OUT} = (\frac{R_U}{R_D} + 1) * V_{CV} * \frac{N_S}{N_A} - VD$$

Here, Ru for the voltage sampling pull-up resistor, Rd for the voltage sampling pull-down resistor; Vcv for the internal voltage reference, typically 4.05V; Ns and Na are the transformer secondary winding turns and auxiliary winding turns; VD is output diode VF.

Through the unique TruePSR™ waveform analysis technology, the output voltage cannot be affected by the load current size to maintain high accuracy.

When the load continues to increase to the maximum operating state of the system but the sampled voltage is still lower than the internal reference voltage, the system will enter the constant current working state.

12.7 Constant current control

When the system enters the constant current output state, the LN1F16/17/18/19/19A/19B will determine the proportional relation of the switching waveform by detecting the time parameter of the VS terminal waveform and keep the demagnetizing time TDIS constant with the switching period by changing the dead time so that the output The current remains at a constant magnitude and the system's maximum demagnetization duty cycle (ratio of demagnetization time to switching period) is 50 %,

$$\frac{T_{DIS}}{T_{ON}+T_D+T_{DIS}}=\frac{T_{DIS}}{T}=0.50$$

TON is the turn-on time; TD is the dead time, the minimum is the main inductor resonant cycle of 1/4, for example 500kHz resonant period, TD is about 0.5us; TDIS for the transformer demagnetization time;

So the output constant current point Iout and the transformer turns ratio Np / Ns and the relationship between the primary peak switch current Ipeak:

$$I_{OUTCC}=0.5*I_{PEAK}*\frac{N_P}{N_S}*0.50$$

For a given system, if the specified flyback voltage or turn ratio, according to the size of the output current constant according to the above formula to obtain the required primary peak switch current Ipeak size:

$$I_{PEAK}=\frac{N_S*I_{OUTCC}}{N_P*0.25}$$

According to the obtained primary peak switch current value, the required current limiting resistance can be calculated according to the following formula:

$$R_{CS}=\frac{V_{CSMAX}}{I_{PEAK}}$$

Here, Vcsmax is the chip maximum current limit threshold, typically 0.75V.

12.8 Frequency control

LN1F16/17/18/19/19A/19B by adjusting the switching pulse time parameters to automatically adjust the switching current size, and the corresponding control of the output state for a specified system, the switching frequency at each moment is result of automatically balancing of the system, so the system switching frequency is the determined by the transformer and the system, when the output current constant according to the requirements of a reasonable set of transformer turns ratio and the system's maximum peak switching current, the maximum switching frequency will be determined by the transformer inductance, the typical maximum switching frequency:

$$F_{MAX}=\frac{2*P_{OUT}}{I_{PEAK}{}^2*L_P*h}$$

Here, Pout is the output constant current point corresponding to the maximum output power; Lp is the transformer primary inductance; η is the conversion efficiency.

The maximum operating frequency of the system should be set reasonably so that it does not exceed the maximum frequency limit (typical value is 70kHz) inside the chip, taking into account the effect of system switching loss and EMI. For general applications, the maximum switching frequency can be set between 35 ~ 60kHz.The recommended value is 55kHz for most applications.

In normal operation, the chip will automatically adjust the switching frequency or switching current according to the load size and input voltage to maintain a good conversion efficiency under various conditions, while avoiding audio noise, the typical switching frequency curve is as follows The figure shows:

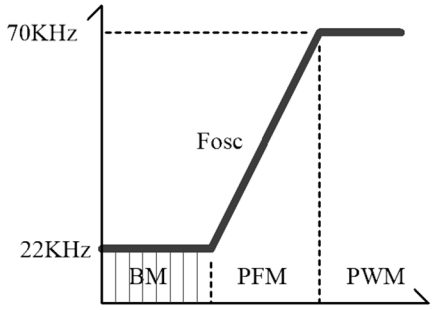


Fig4. Vea VS Fosc curve

12.9 Valley switch control

The LN1F16/17/18/19/19A/19B will set each turn-on action to a fixed position in the resonant period so that the current period can be automatically turned on in a reasonably designed system at the lower voltage position of each resonant waveform (best, the bottom of the resonant trough) Additional low turn-on loss characteristics can be achieved at light load conditions, further improving light-load efficiency.

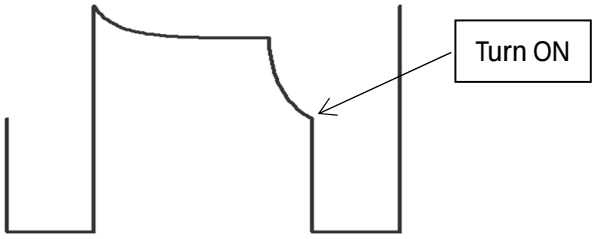


Fig5. valley switch mode

12.10 Startup characteristics

The LN1F16/17/18/19/19A/19B will also ensure that the critical mode is active at every startup, allowing the system to start the process at a lower frequency and automatically increasing the operating frequency as the output voltage increases, so that the start-up does not occur as continuous Current-mode power supply current overshoot problem, which can effectively reduce the impact of starting current to reduce the power switch current stress.

12.11 Output wire voltage drop compensation

The LN1F16/17/18/19/19A/19B features an excellent and easy-to-use output-wire voltage drop compensation technique. The compensation amplitude is set by internal fixed. The output current can be linearly compensated when the output current is increased, thus completely canceling the output The voltage drop generated on the wire to achieve a very precise load voltage regulator output, while the maximum compensation from the internal fixed amplitude of 3.2%, for example, a 5V output system with a maximum compensation voltage of approximately 0.16V.

12.12 Protective function

Excellent power systems require sophisticated fault protection to achieve high reliability. The LN1F16/17/18/19/19A/19B is designed to meet a wide range of user requirements including cycle-by-cycle current limiting (OCP), output overload protection (OLP), VDD overvoltage lockout, and under-voltage lockout (UVLO).

When the VS terminal voltage exceed 5V per unit of time more than twice or the CS voltage exceed 1.45V more than twice

will directly trigger the system into over-voltage protection and overcurrent protection state until the restart.

12.13 Built-in switch and heat treatment

The LN1F16/17/18/19/19A/19B incorporates a high-switching-speed MOSFET power switch with a low RdsON voltage rating of 9/6/4/3/2/1A 650V to maintain low switching losses at switching frequencies as high as 65kHz, yet the chip operation will still produce a certain amount of power Heat, so the application should be carried out in the appropriate heat treatment, a simple approach is to chip in the PIN5/6/7/8 laying enough area of copper foil and tin treatment, as a cooling measures, a typical 18W application of copper foil area should not preferably less than 120 mm^2.

PCB layout should also ensure that high-voltage connection pin and other low-voltage pins or devices to maintain a sufficient safe distance, the minimum safe distance should be at least not less than 1mm is appropriate, so as to avoid damage caused by discharge.

13. Layout Guidelines

13.1 Principles of high-frequency layout

When switching power supply layout should follow the principle of high-frequency layout, where possible, the current loop should be kept to a minimum. It should be advanced and then out of the dual-capacitor and appropriate to maintain a single point of connection capacitance. Three typical current loops are shown in the following figure:

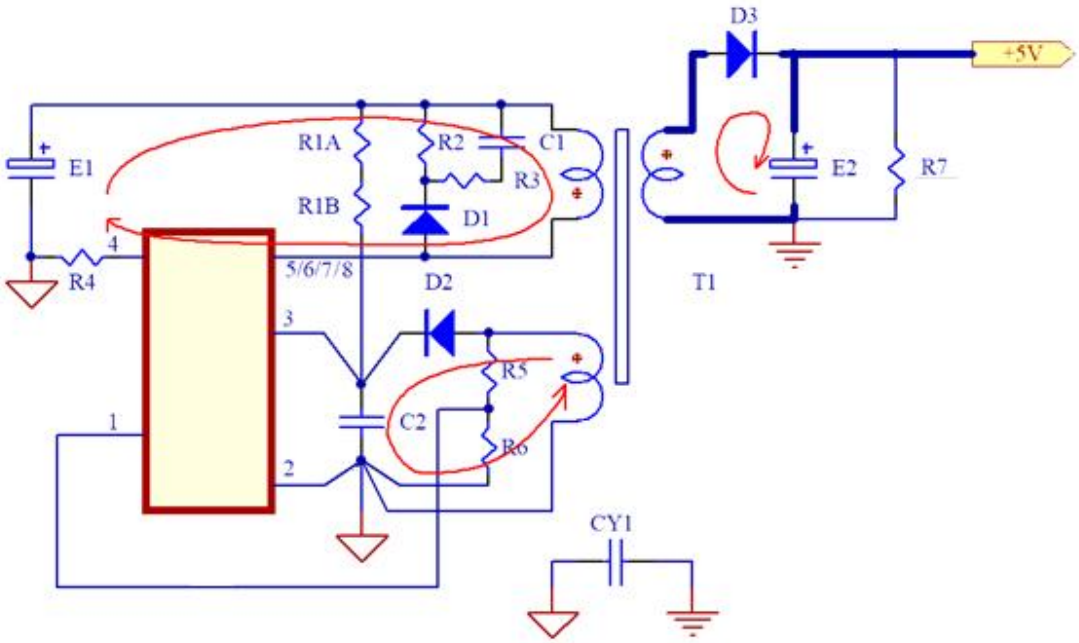


Fig6. Typical current loop diagram

13.2 Typical layout reference

An example of a typical PCB layout is shown below.

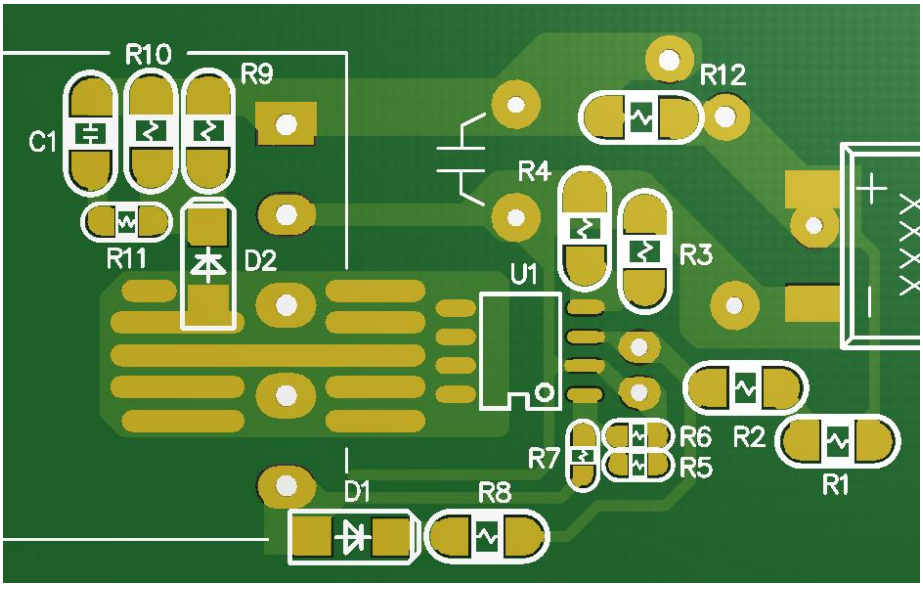


Fig7. Typical layout reference

14. Typical Application Circuit Schematic (input：90~265Vac)

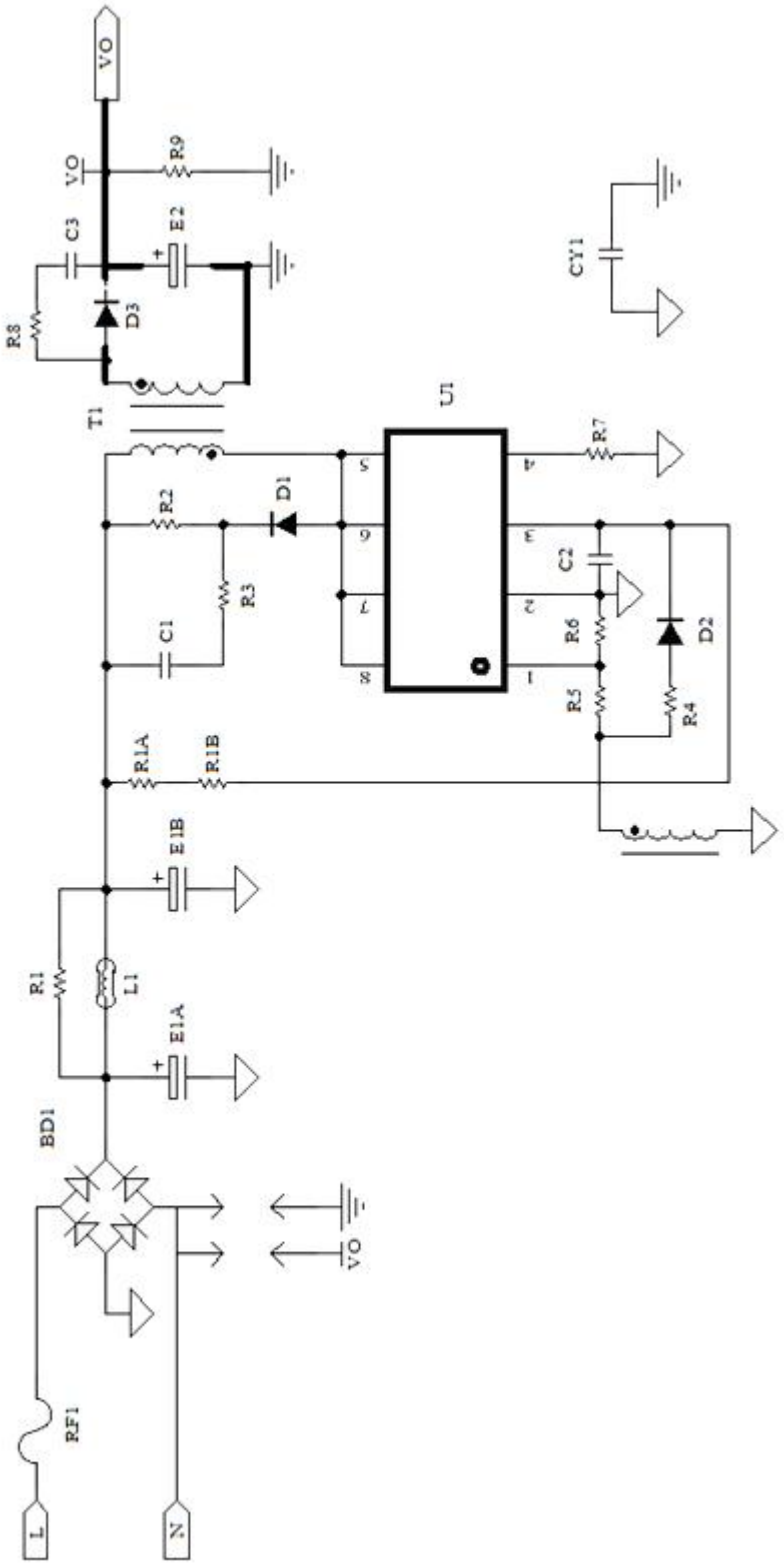
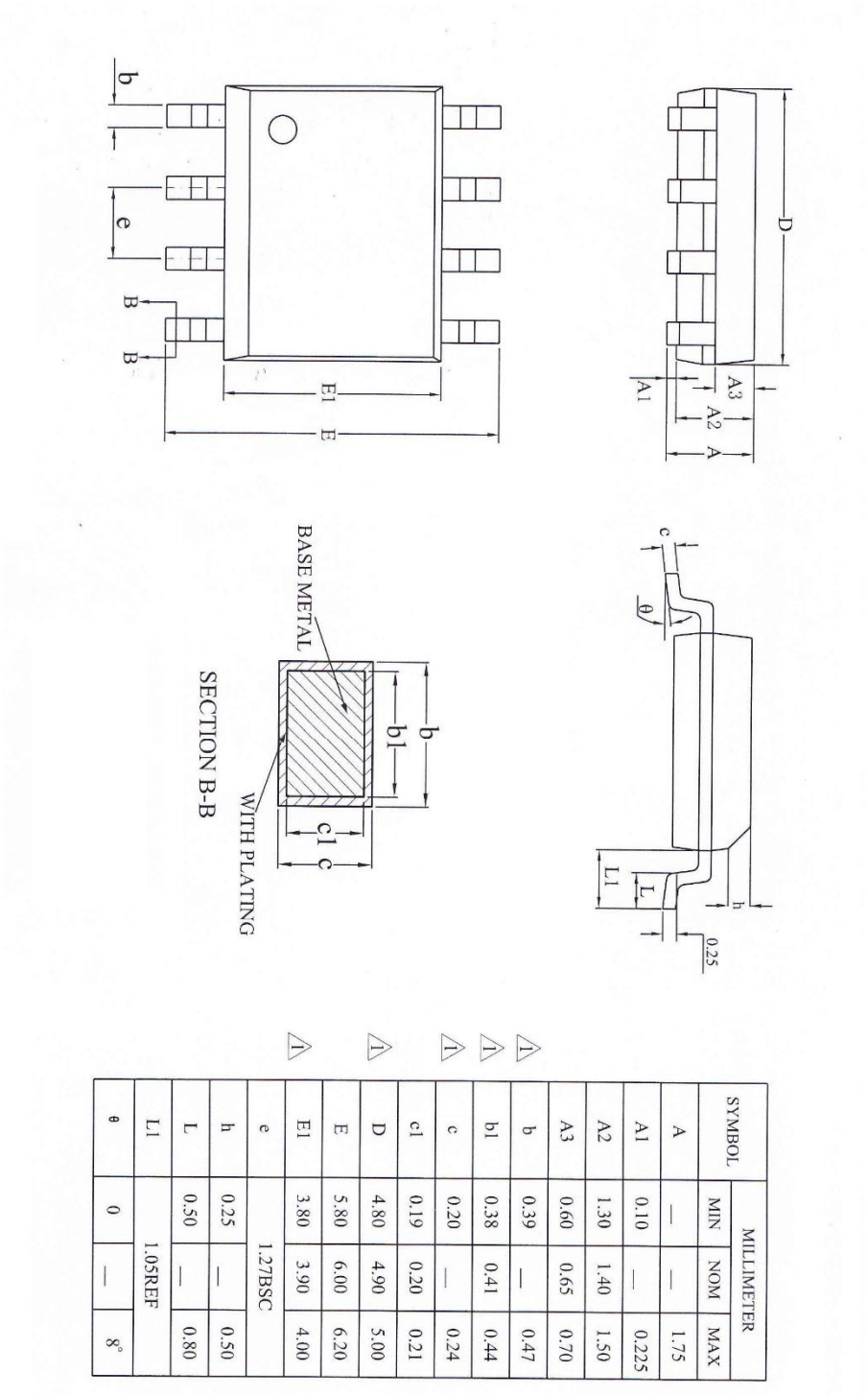


Fig8. Typical Application Circuit Schematic

15. Mechanical and Packaging

SOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Fig9. Mechanical Dimensional Drawings

16. Orderable Information

Part Number	RoHs	B/I MOSFET	Package	Packing
LN1F16	Halogen Free	1A 650V	SOP8	100PCS/TUBE or 4000PCS/REEL
LN1F17		2A 650V		
LN1F18		3A 650V		
LN1F19		4A 650V		
LN1F19A		6A 650V		
LN1F19B		9A 650V		

17. Important Notice

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