

High-performance-PSR-Power-Switch IC

1. Feature

- Built-in TruePSR™ high-precision sampling function
- Built-in 650 V high voltage NMOSFET switch
- Precise primary side regulation accuracy within 2 %
- Precise primary side constant current accuracy within 3 %
- Output voltage drop compensation function with external resistance adjustment
- Low switching loss with full valley switch mode
- Low standby consumption and high energy efficiency to meet the CoC V5 & DoE VI requirements
- No load standby power consumption as low as 50 mW or less
- Built-in CT-PSR™ active cycle turning function
- Low-frequency start-up characteristic control optimizes the starting performance
- Highly reliable low EMI gate drive with soft clamp
- Built-in output over-voltage, short circuit and over-load protection
- Optimized full-range audio-free operation
- Available in TSIP7/TSIP7A package with high power capacity

2. Applications

- Mobile Phone Charger
- Power Adapter
- Battery Charger
- Open-frame Power

3. Description

The LN1F2x is a new generation of high-performance, highly integrated current-mode PSR power switch ICs that can easily build low-standby power consumption, high conversion efficiency, and high performance to meet the energy efficiency standards of CoC V5 and DoE LEVEL VI in applications up to 40 W or more, High-performance PSR primary side of the CC/ CV switching power supply solutions. The chip has built-in high precision constant current and constant voltage control and optimized valley switch technology that provide an output current error of better than ± 3 % accuracy and an output voltage error of ± 2 % accuracy over the full range.

Switching frequencies of up to 70 kHz allow the use of relatively small transformer size to complete the design, while a very small dead-time control allows the system to work in close to critical conduction mode to improve the utilization of the transformer, far superior to traditional PSR controller architecture.

With PWM / PFM / PBM mode multi-segment curve control mode of operation can further optimize the conversion efficiency of system under different loads, especially at light load conversion efficiency, very light load conditions will automatically lock the peak current threshold to maintain efficient conversion, segmented modulation design makes the system with high

conversion efficiency while effectively avoiding audible noise, the standby power consumption can be as low as 50 mW the following.

The low-frequency start-up feature automatically operates once during each power-up and system reset to optimize startup characteristics and to reduce the impact on the high-voltage power switch when switching on and off. Gate drive control with soft clamp further eliminates the risk of driving overvoltage under high supply conditions, while the active gate slope control significantly improves the level of switching interference. The new generation of cycle-rotation technology dedicated to PSR architecture of Lii Semi makes the system extremely EMI-friendly.

The chip can also compensate for the output voltage drop through a specially designed linear output cable voltage drop compensation adjustment pin to improve the accuracy of the output voltage under load and maintain accurate load voltage from the load.

LN1F2x also provides a very complete protection circuit with automatic recovery, including cycle-by-cycle current limit (OCP), with high and low voltage compensation output over-current protection (OCP), VDD over-voltage protection and under voltage lockout (UVLO) .

Now halogen-free TSIP7/TSIP7A package that meet RoHS requirements is available.

4. Functional Block Diagram

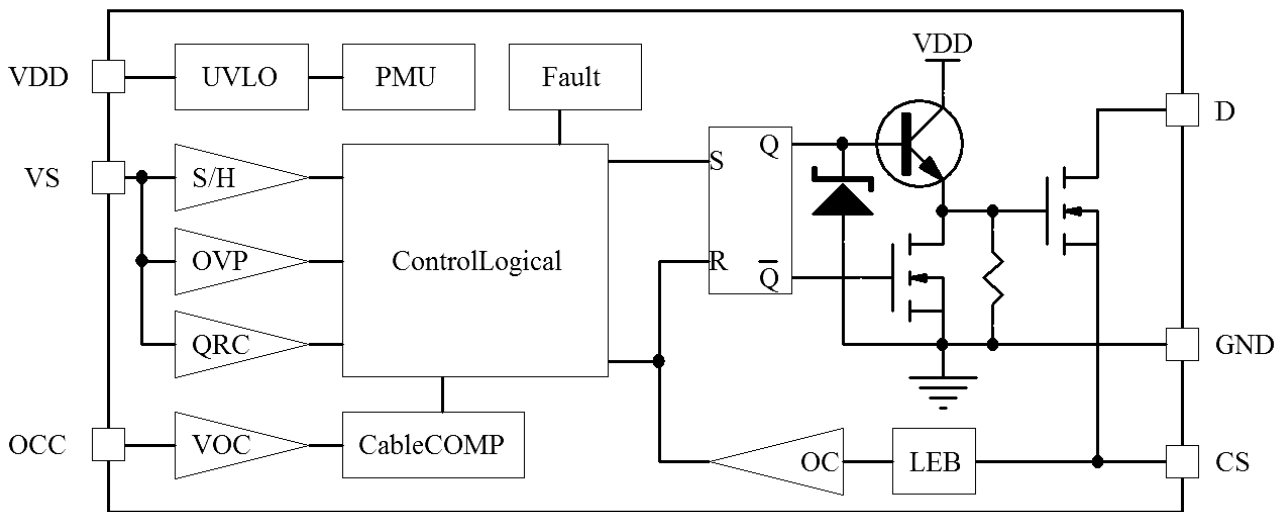


Fig1. Internal functional block diagram

5. Pin Definitions

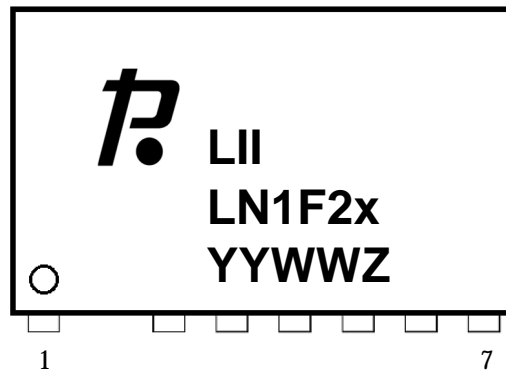


Fig2. Pin Definitions

6. Pin Function Description

PIN	Symbol	Function
1	D	The high-voltage MOSFET switch's drain output pin, which connects the transformer
2	VDD	Power supply pin, connect the starting resistor and auxiliary power supply circuit
3	CS	Switch current sense signal input pin, connected to the current sense resistor
4	GND	Ground pin
5	VS	Output voltage and switch signal detection pin, connected to the feedback sampling network
6	OCC	Output Cable voltage-drop Compensation adjustment pin, connect the set resistance
7	NC	Not connected pin, unused, can be left floating or grounded in the application or other pins except pin D

7. Typical Simplified Schematic

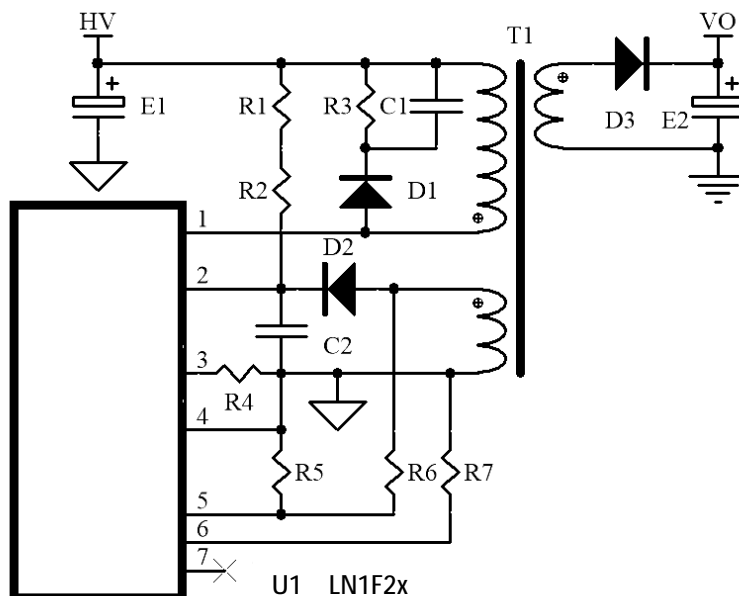


Fig3. Typical Simplified Schematic

8. Absolute Maximum Ratings *

Parameter		Rating	Units
D Pin Voltage		650**	V
VDD Pin Voltage		30***	V
Other Pin Voltage		-0.3 to +7	V
D Pin Current	LN1F24	4****	A
	LN1F26	7****	A
	LN1F28	10****	A
Min/Max Operating Junction Temperature T _J		-40 to +150	°C
Min/Max Operating Ambient Temperature T _a		-20 to +105	°C
Min/Max Storage Temperature T _{stg}		-55 to +150	°C
PD		2200	mW
ESD	HBM	2500	V
	MM	250	V

Note*: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.** : with 1mA limit. *** : with 10mA limit. ****: For test, Pulse width is 1ms and cycle is 1S.

9. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
D	Drain Peak Voltage	-	-	600	V
VDD	VDD Supply Voltage	10		25	V
TA	Operating Ambient Temperature	-20		85	°C

10. Electrical Characteristics(Ta = 25°C, VDD=15V, if not otherwise noted)

MOSFET Section (D Pin)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV _{DSS}	Drain-Source Voltage	VDD=0 V, I _D =1 mA	650	700		V
I _{HV}	D-S Leakage Current	V _D =650 V			10	uA
R _{DS(ON)}	MOSFET R _{ds(ON)}	LN1F24, I _D =1.4 A, T _J =25 °C		2.20		Ω
		LN1F26, I _D =2 A, T _J =25 °C		1.35		Ω
		LN1F28, I _D =3.5 A, T _J =25 °C		0.85		Ω
T _R	Switch Rise Time	CL=0.5 mH		50		nS
T _F	Switch Fall Time	CL=0.5 mH		50		nS
I _D	Drain Current Pulsed	T _J =25 °C, LN1F24		4		A
		T _J =25 °C, LN1F26		7		A
		T _J =25 °C, LN1F28		10		A
		T _J =105 °C, LN1F24		1.8		A
		T _J =105 °C, LN1F26		3		A
		T _J =105 °C, LN1F28		5		A

VDD Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I _{OS}	VDD Startup Current	VDD=20 V	-	1	10	uA
I _O	Operating Current	VDD=25 V ÷ 16 V, VFB=OPEN	-	0.5	-	mA
V _{STOP}	UVLO Threshold Voltage	VDD=25 V ÷ 0 V	7.8	8.8	9.8	V
V _{START}		VDD=0 V ÷ 25 V	-	21	-	V
V _{OVP}	VDD OVP Threshold	I _{VDD} =5 mA	-	27.5	-	V
VDD_CL	VDD Clamp Voltage	I _{VDD} =10 mA	-	30	-	V

VS Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V _{CV}	VS Reference Voltage			4.05		V
V _{VS(OVP)}	VS OVP Threshold			4.5		V

OCC Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V _{OCCMIN}	Min. OCC Voltage	OCC=OPEN		0		V
V _{OCCMAX}	Max. OCC Voltage	OCC=0 V, V _{out} =5 V		0.45		V
G _{OCCMAX}	Max. OCC Scale	Load=Max. load		9		%
V _{OCC}	OCC Open Voltage	OCC=OPEN		3		V

CS Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
T _{LEB}	L.E.B Time		-	250	-	nS
Z _{CS}	CS Input Resistance		-	40	-	KΩ
T _{CS}	CS Delay Time	VDD=16 V, V _{CS} >V _{TH_OC}	-	75	-	nS
V _{CSMAX}	Max. CS Threshold		-	0.75	-	V
V _{CSMIN}	Min. CS Threshold		-	0.20	-	V
V _{CSOSP}	OSP Threshold voltage	OSP>2 Cycle	-	1.45	-	V

OSC Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F _{OSC}	Switching Frequency		22		65	KHz
F _{OSCMIN}	Min. Switching Frequency			350		Hz
ΔF _{OSC_T}	F _{OSC} VS Ta	VDD=16 V, Ta=-20 °C to 100 °C		5		%
ΔF _{OSC_V}	F _{OSC} VS VCC	VDD=12-25 V		5		%
D _{Max}	Max. Duty			50		%
T _{OFFMIN}	Min. Discharge Time			2		us

Cycleturning™II (C.T.PSR) Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ΔF _{OSC}	C.T. Range		-2		+2	%
T _{CT}	C.T. Time		-	4	-	mS

OTP Section

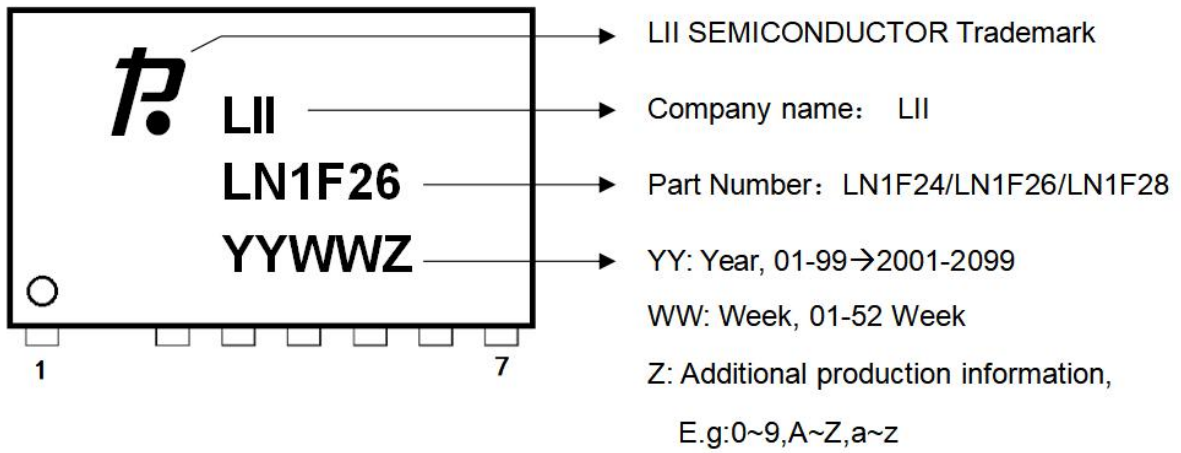
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{OTP}	OTP Threshold	VDD=16 V		150		°C
t_{OTPHYT}	OTP Hysteresis	VDD=16 V		30		°C

Thermal Data

Symbol	Parameter	Rating	Unit
θ_{JA}^1	Thermal Resistance Junction-Ambient	60	°C/W
θ_{JC}^2	Thermal Resistance Junction-Case	12	°C/W

Notes: 1. All leads are soldered on a 250 mm² copper foil with 2 oz thick to measuring. 2. Measured on the surface of the package near pin 1.

11. Marking Information.



12. Application and Implementation

The LN1F2x is a highly integrated, constant-current, constant-voltage PSR controller IC with built-in high voltage power MOSFET. Its highly efficient BM and valley switch hybrid mode control significantly reduces standby losses, improves conversion efficiency at light loads, and easily meets international energy efficiency standards such as CoC V5 and DoE LEVEL VI.

12.1 Start-up current and start-up control

The LN1F2x can operate at very low start-up current conditions, with accurate UVLO control enabling fast and reliable power-up in a short period of time. Allowing a large start-up resistor value can significantly reduce the start-up power consumption, such as 6 M Ω , although a 1/8W power-class resistor can meet the required power requirements, but must still carefully consider its ability to withstand voltage, The use of resistors in series is recommended, for example, using two 1206-type chip resistors in series.

The start-up resistor can be connected between AC input terminal or the positive of input DC high voltage and the VDD storage capacitor. When the VDD voltage is charged to 21 V after power-on, the internal circuit is started and the output drive pulse is finally set to the internal MOS GATE terminal, the system work begins.

12.2 Operating current and VDD capacitance

The normal operating current of LN1F2x is as low as 0.5 mA. The loss of the IC itself is small during operation. An electrolytic capacitor with capacity of not less than 4.7 μ F can meet the sufficient energy required for IC power supply and driving, but consider the larger input capacitance of MOSFET and the wider operating temperature range, a lower internal resistance (ESR) type of the capacitor should be chosen to provide fast and large current when the MOSFET is turned on, speeding up MOSFET turn-on, in a typical system design recommended 4.7 μ F capacitor as VDD capacitance. In order to meet the VDD range under the maximum operating conditions, the capacitor withstand voltage should be not less than 35 V is appropriate. A non-polar capacitor should be connected in parallel near to the VDD and GND pins, the capacity should be not less than 100 nF is appropriate.

12.3 Cycleturning™ PSR (C.T. PSR)

The LN1F2x integrates the second-generation CycleTurning™ proprietary technology from Lii Semi optimized for PSR that the clock cycle is modulated(CT-PSR) at the set time in the work process, resulting in a larger switching pulse spectrum to reduce the narrowband energy density, so that the average interference intensity in any single bandwidth is greatly reduced. Therefore, the cost of the system on EMI is also greatly reduced.

12.4 Extended BM operating characteristics

Under no-load or light-load conditions, the ratio of the total loss of MOSFET switching losses will increase significantly, and the switching loss is proportional to the switching frequency. Lowering the switching frequency can significantly reduce the switching losses of the MOSFET. LN1F2x by detecting the VS voltage and time size, the system no-load or light load will automatically adjust the switching frequency to a lower value, the more internal modulation voltage is lower than the set

control voltage, the more the frequency decreases, but the circuit automatically limits the minimum value of the frequency drop above 22 kHz to avoid audible noise.

When the system frequency drops to near 22 kHz, if the modulation voltage is still lower than the set control voltage, the output will be disabled to ensure that the output voltage will not be too high, then the system will enter the BM mode to avoid audio noise, And as the load continues to reduce the number of pulses until the pulse into a single state, in order to optimize the system dynamic load response performance, the system will automatically lock the lowest equivalent switching frequency of 350 Hz. The minimum load required should be applied in the application to avoid the system being reduced to the minimum frequency to prevent the output voltage from flying high during no-load, and sufficient margin should be maintained.

12.5 Current detection and leading edge blanking

The LN1F2x provides cycle-by-cycle current limiting, and the switching current is sampled into the IC through the current limiting resistor. The built-in leading-edge blanking eliminates current spikes into the IC, avoid the current limit function malfunction, the MOSFET will not be turned off by mistake, so the traditional external blanking circuits will no longer be needed.

The maximum current limit threshold, the current comparator's maximum threshold voltage, is 0.75 V.

12.6 Constant voltage control

LN1F2x by sampling the voltage waveform on the auxiliary winding, through a series of internal sampling chip, keep, analyze, deal with, produce the required various signals. Which compares the voltage signal with the internal reference voltage to generate a voltage error signal and adjusts the switch state according to the voltage error signal so as to compensate for changes in output voltage caused by an increase or decrease in output load and an increase or decrease in input voltage, The typical output voltage (V_{OUT}) is:

$$V_{OUT} = \left(\frac{R_U}{R_D} + 1\right) * V_{CV} * \frac{N_S}{N_A}$$

Here, R_U for the voltage sampling pull-up resistor, R_D for the voltage sampling pull-down resistor; V_{CV} for the internal voltage reference, typically 4.05 V; N_S and N_A are the transformer secondary winding turns and auxiliary winding turns.

Through the unique TruePSR™ waveform analysis technology, the output voltage cannot be affected by the load current size to maintain high accuracy.

When the load continues to increase to the maximum operating state of the system but the sampled voltage is still lower than the internal reference voltage, the system will enter the constant current working state.

12.7 Constant current control

When the system enters the constant current output state, the LN1F2x will determine the proportional relation of the switching waveform by detecting the time parameter of the VS terminal waveform and keep the demagnetizing time T_{DIS} constant with the switching period by changing the dead time so that the output The current remains at a constant magnitude and the system's maximum demagnetization duty cycle (demagnetization time to switching period ratio) is 50 %,

$$\frac{T_{DIS}}{T_{ON} + T_D + T_{DIS}} = \frac{T_{DIS}}{T} = 0.50$$

T_{ON} is the turn-on time; T_D is the dead time, the minimum value is the main inductor resonant cycle of 1/4, for example, for a 500 kHz resonant period, T_D is about 0.5 us; T_{DIS} for the transformer demagnetization time;

So the output constant current point I_{OUT} and the transformer turns ratio N_P / N_S and the relationship between the primary peak switch current I_{PEAK} is:

$$I_{OUTCC} = 0.5 * I_{PEAK} * \frac{N_P}{N_S} * 0.50$$

For a given system, if the specified flyback voltage or turn ratio, according to the above formula, the required primary peak switching current I_{PEAK} can be obtained according to the required output constant current value:

$$I_{PEAK} = \frac{N_S * I_{OUTCC}}{N_P * 0.25}$$

According to the obtained primary peak switch current value, the required current limiting resistance can be calculated according to the following formula:

$$R_{CS} = \frac{V_{CSMAX}}{I_{PEAK}}$$

Here, V_{CSMAX} is the chip maximum current limit threshold, typically 0.75 V.

12.8 Frequency control

LN1F2x automatically adjusts the switch current by adjusting the time parameter of the switch pulse, and controls the output state accordingly. For a specified system, the switching frequency at each moment is the result of automatic balancing of system. Therefore, the system switching frequency is determined by the transformer and the system. When the ratio of the transformer and the maximum peak switching current of the system are properly set according to the output constant current requirement, the maximum switching frequency will be determined by the transformer inductance, the typical maximum switching frequency:

$$F_{MAX} = \frac{2 * P_{OUT}}{I_{PEAK}^2 * L_P * \eta}$$

Here, P_{out} is the maximum output power corresponding to the output constant current point; L_P is the transformer primary inductance; η is the conversion efficiency.

The maximum operating frequency of the system should be reasonably set so as not exceed the maximum frequency limit (typical value is 65 kHz, maximum value is about 70 kHz) inside the chip, taking into account the effect of system switching loss and EMI. For general applications, the maximum switching frequency can be set between 35~65 kHz.

In normal operation, the chip will automatically adjust the switching frequency or switching current according to the load size and input voltage level, so as to maintain good conversion efficiency under various conditions, while avoiding audio noise.

The typical switching frequency curve is as follows the figure shows:

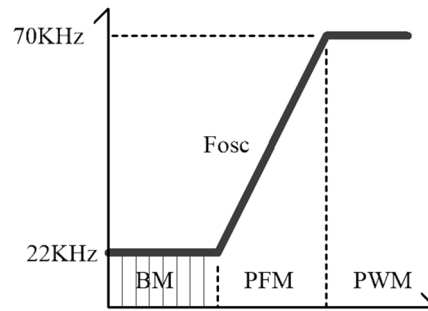


Fig4. V_{ea} VS F_{osc} curve

12.9 Valley switch control

The LN1F2x will set each turn-on action to a fixed position in the resonant period so that the current period can be automatically turned on in a reasonably designed system at the lower voltage position (best, the bottom of the resonant trough) of each resonant waveform. Additional low turn-on loss characteristics can be achieved at light load conditions, further improving light-load efficiency.

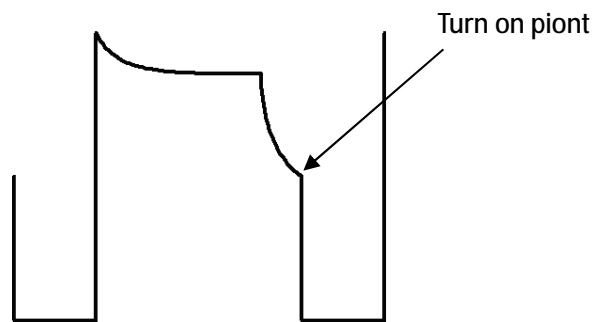


Fig5. Valley switch mode

12.10 Startup characteristics

The LN1F2x will ensure that the critical mode is valid at each startup, which allows the system to start the process at a lower frequency and automatically increase the operating frequency as the output voltage rises, so that the start-up current overshoot problem like the continuous current mode power supply does not occur during startup, which can effectively reduce start current surge to reduce power switch current stress.

12.11 Output wire voltage drop compensation

The LN1F2x features an excellent and easy-to-use output-wire voltage drop compensation technique. The compensation amplitude can be set by a simple external resistor. The output voltage can be linearly compensated in real-time when the output current is increased, thus completely canceling the voltage drop generated on the output wire to achieve a very precise load voltage regulated output, while the maximum compensation amplitude is fixed internally by the IC to 9% , For 5V , is 0.45 V.

The ratio of the typical compensation voltage, V_{occ} , to the output voltage, V_{OUT} , is K_{occ} :

$$k_{OCC} = \frac{V_{OCC}}{V_{OUT}} = \frac{2315}{R_{OCC} + 28000}$$

R_{OCC} is the external compensation resistance in Ω .

12.12 Protective function

Excellent power systems require sophisticated fault protection to achieve high reliability. The LN1F2x is designed with a wide range of protection features to meet user requirements including cycle-by-cycle current limiting (OCP), output overload protection (OLP), VDD overvoltage lockout, and under-voltage lockout (UVLO).

When the VS terminal voltage exceeds 4.5 V more than twice per unit time or the CS voltage exceeds 1.45 V more than twice, it will directly trigger the system into over-voltage protection and over-current protection state until restart.

12.13 Built-in switch and heat treatment

The LN1F2x incorporates a low R_{dsON} high-switching-speed MOSFET power switch with voltage rating up to 4A/7A/10 A and 650 V to maintain low switching losses at switching frequencies as high as 65 kHz, yet the chip operation will still produce a certain amount of power Heat, so the application should be carried out in the appropriate heat treatment, a simple approach is to chip in the PIN 1 laying enough area of copper foil and tin treatment, as a cooling measures, a typical 20 W application of copper foil area should not preferably less than 150 mm². In more powerful applications, sufficient independent heat sinks should be applied as a means of heat dissipation to keep the IC temperature within the allowable range.

PCB layout should also ensure that high-voltage connection pin and other low-voltage pins or devices to maintain a sufficient safe distance, the minimum safe distance should be at least not less than 1 mm is appropriate, so as to avoid damage caused by discharge.

13. Layout Guidelines

13.1 Principles of high-frequency layout

When switching power supply layout should follow the principle of high-frequency layout, where possible, the current loop should be kept to a minimum. It should be advanced and then out of the dual-capacitor and appropriate to maintain a single point of connection capacitance. Three typical current loops are shown in the following figure:

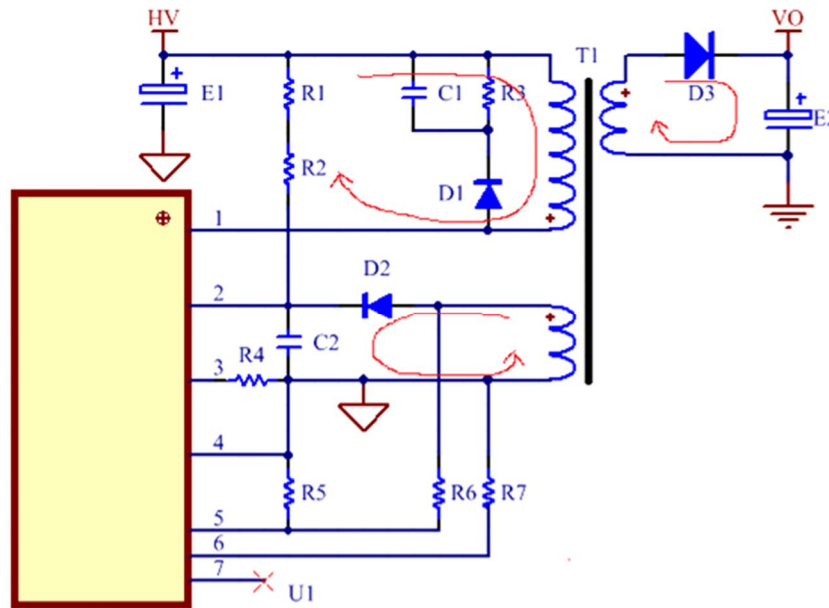


Fig6. Typical current loop diagram

13.2 Typical layout reference

An example of a typical PCB layout is shown below.

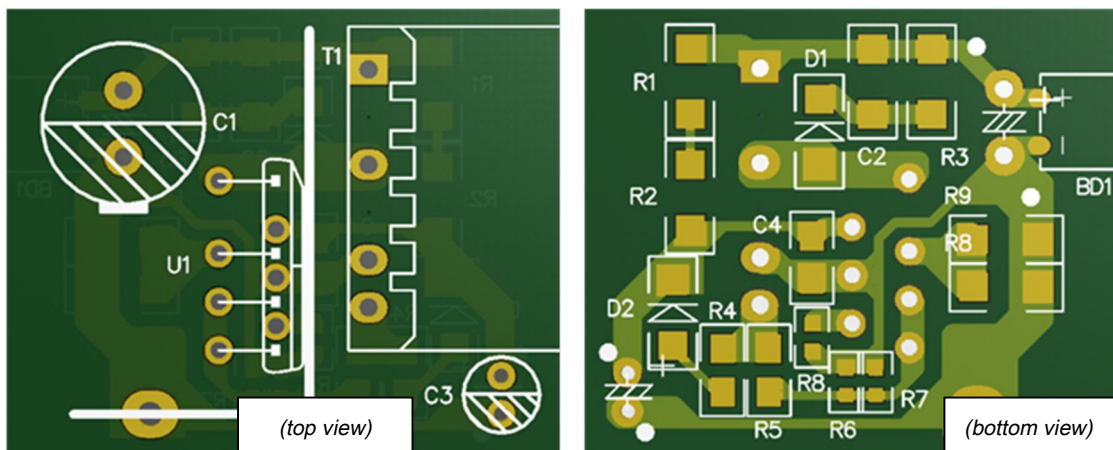
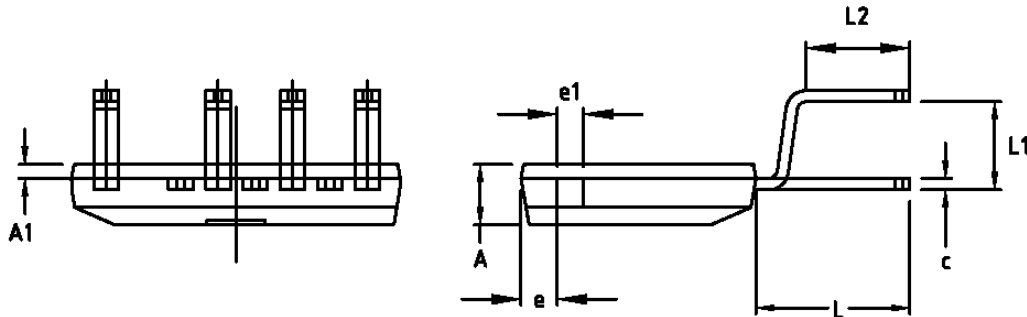


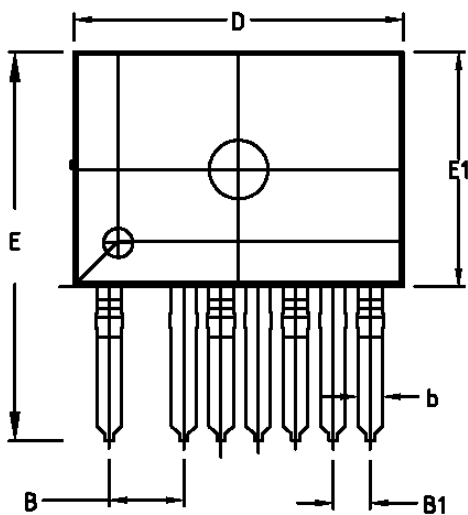
Fig7. Typical layout reference

15. Mechanical and Packaging

TSIP7



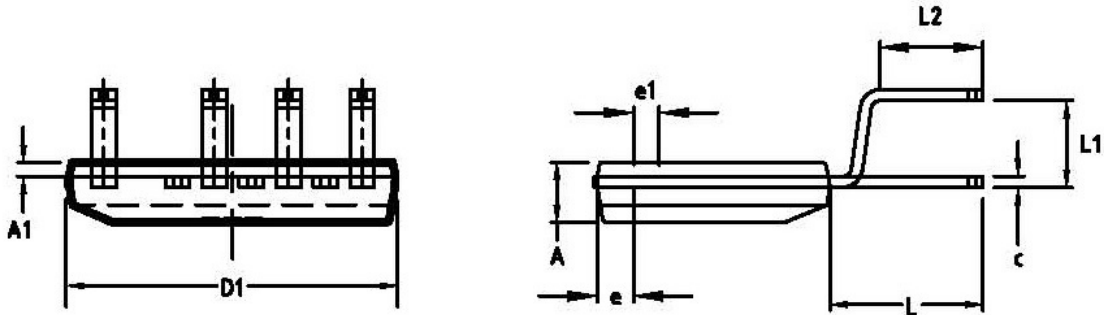
Note: All dimension are in millimeter



SYMBOL	MIN	NOM	MAX
A	1.96	2.06	2.16
A1	0.43	0.48	0.53
b	0.80	0.84	0.89
B	2.44	2.54	2.64
B1	1.17	1.27	1.37
c	0.38	0.38	0.40
D	11.00	11.20	11.30
E	13.05	13.25	13.45
E1	7.80	8.00	8.20
e	0.50	0.60	0.70
e1	0.32	0.37	0.42
L	5.05	5.25	5.45
L1	2.80	3.00	3.20
L2	3.50	3.70	3.90

Fig9. Mechanical Dimensional Drawings(mm)

TSIP7A



Note: All dimension are in millimeter


SYMBOL	MIN	NOM	MAX
A	1.96	2.06	2.16
A1	0.43	0.48	0.53
b	0.70	0.75	0.80
b1	0.77	0.82	0.87
b2	0.45	0.50	0.55
b3	0.87	0.92	0.97
b4	0.79	0.84	0.89
B	2.44	2.54	2.64
B1	1.17	1.27	1.37
c	0.38	0.38	0.40
D	11.00	11.20	11.40
D1	11.00	11.40	11.80
E	11.75	12.75	13.75
E1	7.80	8.00	8.20
e	0.50	0.60	0.70
e1	0.32	0.37	0.42
L	4.55	4.75	4.95
L1	2.80	3.00	3.20
L2	2.54	3.04	3.54

Fig10. Mechanical Dimensional Drawings(mm)

16. Orderable Information

Part No.	MOSFET RdsON	MOSFET BVdss	Package	Quantity per Tube
LN1F24	2.20	650 V	TSIP7 TSIP7A	45 PCS/TUBE
LN1F26	1.35			45 PCS/TUBE
LN1F28	0.85			45 PCS/TUBE

17. Important Notice

力生美、Lii semi、 等均为力生美半导体的商标或注册商标，未经书面允许任何单位、公司、个人均不得擅自使用，所发布产品规格书之著作权均受相关法律法规所保护，力生美半导体保留全部所有之版权，未经授权不得擅自复制其中任何部分或全部之内容用于商业目的。

产品规格书仅为所描述产品的特性说明之用，仅为便于使用相关之产品，力生美半导体不承诺对文档之错误完全负责，并不承担任何因使用本文档所造成的任何损失，本着产品改进的需要，力生美半导体有权在任何时刻对本文档进行必要的修改，并不承担任何通知之义务。英文规格书皆由中文规格书翻译而来，相关内容均以中文规格书为准。

力生美半导体系列产品均拥有相关技术之自主专利，并受相关法律法规保护，未经授权不得擅自复制、抄袭或具有商业目的的芯片反向工程，力生美半导体保留相关依法追究之权利。

力生美半导体不对将相关产品使用于医学、救护等生命设备所造成的任何损失承担责任或连带责任，除非在交易条款中明确约定。

最新信息请访问：

www.liisemi.com